

Ghost Processor

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Report

Aim: To build a basic 4-bit processor using Verilog which performs basic operations like addition, subtraction, multiplication, shifting bits, etc.

Tools used: Xilinx, Isim Simulator

Modules Used:

1. 10 bit adder
2. Addition & subtraction module
3. 4 bit and/or/not gate
4. Arithmetic right shift
5. Booth Multiplication
6. Carry Lookahead adder
7. Circular left/right shift
8. Counter

9. Decoder 2 to 4 & 4 to 16
10. Increment by $1/k$
11. Decrement by 1
12. D Flip Flop
13. Encoder 2 to 4
14. Left/Right Shift
15. Mux 2-1, 4-1, 8-1, 16-1 (1 and 4 bit)
16. Register

Description of each module:

Addition & subtraction module:

Addition and subtraction module uses carry look ahead adder for both addition and subtraction based on a bit addsub. Subtraction is similar to doing two's complement of second number and then adding it to first number.

4 bit and/or/not gate:

4-bit and/or/not gates are implemented by doing and/or/not of each bit.

Arithmetic right shift:

Arithmetic right shift is similar to normal right shift but MSB of answer bit retains the MSB of

number to be shifted. Useful in booth's multiplication.

Carry Look Ahead adder:

Carry look ahead adder generates carry for each block of addition using propagation(p) and generation(g). The recursive equation for carry is $c(i+1) = x(i)y(i) + x(i)c(i) + y(i)c(i)$ and each sum bit is generated using Xor.

$$s(i) = x(i) \text{ xor } y(i)$$

Circular left/right shift: circular left shift retains the last bit into LSB of answer without removing it. Circular right shift retains first bit into MSB of answer.

Counter: A basic 2-bit counter is implemented using D-Flip Flop having a clear bit also as input. It counts the clock cycles at each posedge. Clear resets the counter to 00.

Decoder 2 to 4 & 4 to 16: Decoder decodes the given binary representation of number into one-hot representation where only one of the

outputs is active. It helps in designing the control unit of processor.

Increment by 1/k: Increment uses carry lookahead adder to add 1'b1 or k to the input.

Decrement by 1: Subtracts 1 using the same carry lookahead adder.

Encoder 2 to 4: Encoder encodes the given one-hot representation to binary number.

Left/Right Shift: Left shift shifts the given input by k spaces to the left adding 0's to the right.

Mux 2-1, 4-1, 8-1, 16-1: Multiplexer implements the output as one of the given input based on selection bit.

Design of Control Unit:

Control unit is the basic unit which generates control signals for the whole modules and function of processor. It generates signals

whether registers should accept inputs(R in), give outputs to bus(R out), Functions giving values into bus(Fn), inputs and outputs from temporary registers(A in, A out, G out), external input(extern 2bit, extern 4bit), clear for counter(clear), Input instructions decoding(I), decoded counter of cycles(T) .

Integration of all units(main):

All units i.e. registers, function modules, control unit are assembled using the system of buses. Two buses , one for input and one for output are used. To input bus all the inputs of registers and function outputs are connected. To output bus all the outputs of registers and inputs of function modules are connected. To ensure that at any instant only one of the function modules and registers is connected to any bus we use mux 16:1 and the control bits for this are generated by encoding the instruction bits(I). The same method is used for carry and overflow bits generated at every function module.